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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,781	12/07/2000	Davide Patti	854063.601	2944

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 01/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/733,781	Applicant(s) PATTI	
	Examiner Matthew E. Warr n	Art Unit 2815	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 20-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 20-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Amendment filed on November 5, 2002.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "said insulation region" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito (JP 06-342878 A).

Ito discloses (abstract and fig. 1) an integrated circuit device comprising a high voltage resistor (R) integrated in a semiconductor material body (12) in which the resistor has a vertical current flow. The resistor has the same conductivity type (N) as

the semiconductor material body and is formed by a portion of the semiconductor material body extending between a first (top) surface (14) and second (bottom) surface (10) of the body.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (JP 06-342878 A) as applied to claim 1 above, and further in view of Sakai et al. (JP 61-232657 A).

Ito shows all of the elements of the claims except the resistor delimited at least partially by an insulation region extending from the first surface towards a second surface. Sakai et al. discloses (abstract and fig. 1 on page 3) an integrated circuit device comprising a high voltage resistor (R) integrated in a semiconductor material body (3). The resistor has the same conductivity type (N) as the semiconductor material body and is formed by a portion of the semiconductor material body extending between a first (top) surface and second (bottom) surface of the body. The resistor is delimited at least partially by an insulation region (11) extending from the first surface towards the second surface of the body. The insulating region has a closed shape and is formed of isolating material. A first and second region (regions 5 on each side of insulator 11)

having a conductivity type opposite (P) that of the material body is arranged on opposite sides of the insulation region. This configuration helps increase the electrostatic breakdown capacity. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the vertical resistor Ito by forming the resistor between two isolation regions as taught by Sakai to increase the electrostatic breakdown capacity of an ESD device.

Claims 20-23 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (JP 06-342878 A) in view of Sakai et al. (JP 61-232657 A).

Ito discloses (abstract and fig. 1) an integrated circuit device comprising a high voltage resistor (R) integrated in a semiconductor material body (12) in which the resistor has a vertical current flow. The resistor has the same conductivity type (N) as the semiconductor material body and is formed by a portion of the semiconductor material body extending between a first (top) surface (14) and second (bottom) surface (10) of the body. Ito shows all of the elements of the claims except the resistor delimited at least partially by an insulation region extending from the first surface towards a second surface. Sakai et al. discloses (abstract and fig. 1 on page 3) an integrated circuit device comprising a high voltage resistor (R) integrated in a semiconductor material body (3). The resistor has the same conductivity type (N) as the semiconductor material body and is formed by a portion of the semiconductor material body extending between a first (top) surface and second (bottom) surface of the body. The resistor is delimited at least partially by an insulation region (11) extending from the

first surface towards the second surface of the body. The insulating region has a closed shape and is formed of isolating material. A first and second region (regions 5 on each side of insulator 11) having a conductivity type opposite (P) that of the material body is arranged on opposite sides of the insulation region. First and second electronic devices (Q1 and Q2 [not shown in fig. 1]) are formed on opposite sides of the insulation region. The insulating region is open at a bottom portion such that the semiconductor region (3) is contiguous with the semiconductor body (1). The semiconductor region has a rectangular cross section and the insulating region has a rectangular frame shape. The semiconductor region (3) includes an upper region (6) adjacent to the surface of the semiconductor body and a lower region (3) below the upper region, wherein the upper region is doped at a higher doping level (n+) than the lower region (n). The semiconductor region also includes an upper region (5) adjacent to the surface of the semiconductor body and a lower region (2) positioned below the upper region, wherein the upper region has a conductivity type (p) opposite to the conductivity type (n)of the lower region, inherently forming a diode. This configuration helps increase the electrostatic breakdown capacity. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the vertical resistor Ito by forming the resistor between two isolation regions as taught by Sakai to increase the electrostatic breakdown capacity of an ESD device.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (JP 06-342878 A) in view of Sakai et al. (JP 61-232657 A) as applied to claim 20 above, and further in view of Sivan (US 5,229,310).

Ito in view of Sakai et al. shows all of the elements of the claims except the insulating region having conductive filler surrounded by insulating walls. Sivan shows (fig. 1F) a semiconductor device having a trench lined with insulating material (32) and conductive filler (38) surrounded by the insulating walls. The region also includes an upper region (28) of a first conductivity type, a middle region of a second conductivity type, and lower region (26) also of the first conductivity type. The upper and lower regions operate as source/drain regions and the conductive material (38) functions as a gate electrode (col. 5, lines 12-21 and col. 6, lines 11-30). This configuration minimizes the transistor size and ultimately increases the cell density. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulation region of Ito and Sakai by filling the layer with conductive material as a gate as taught by Sivan to reduce the transistor size and increase the cell density.

Response to Arguments

Applicant's arguments with respect to claims 1-7 and 20-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW

January 23, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800